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10/064,157	06/14/2002	John Gildred	PR 1800.01 U	5100

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EXAMINER	
AUSTIN, SHELTON W	
ART UNIT	**PAPER NUMBER**
2112	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/064,157	GILDRED, JOHN	
	Examiner	Art Unit	
	Shelton Austin	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/08/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-5 and 7-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Ezer et al. (US 6,275,239, hereinafter '239).

In regards to claim 1, '239 teaches a three-dimensional output system (Figs. 1-4—102) comprising: a hardware decoder (Fig. 4—201) that receives live broadcast signals and outputs video frames; a three-dimensional graphics chip (Fig. 2 & 4—203; Fig. 3—330a; col. 7, lines 39-41) having a texture memory (Fig. 4—425; col. 8, lines 12-44) that transforms said video frames to three-dimensional graphics frames and outputs said three-dimensional graphics frames to an output device (fig. 3—310); and a transport mechanism (Fig. 4—202, 401, & 402) that obtains said video frames from said decoder and transports said frames to said texture memory of said three-dimensional graphics chip.

In regards to claim 3, '239 teaches the system of claim 1 wherein said transport mechanism comprises a PCI bus (Fig. 4—40-2).

In regards to claim 4, '239 teaches the system of claim 1 wherein said output device is a television set (col. 4, lines 42-43).

In regards to claim 5, '239 teaches the system of claim 1 wherein said output device is a monitor (col.4, lines 42-46).

In regards to claim 7, '239 teaches the system of claim 1 wherein said hardware decoder, said three- dimensional graphics chip, and said transport mechanism reside in a set-top box (col. 3, lines 10-14).

In regards to claim 8, '239 teaches the system of claim 7 wherein said hardware decoder, said three-dimensional graphics chip, and said transport mechanism are all components of a single chip (col. 1, lines 62-65; col. 3, line 57-col. 4, line 35).

In regards to claim 9, '239 teaches the system of claim 7 wherein said hardware decoder, said three- dimensional graphics chip, and said transport mechanism are all components on separate chips (col. 1, lines 41-59).

In regards to claim 10, '239 teaches the system of claim 1 wherein said transport mechanism transports said frames to said texture memory from said decoder using a direct memory address (DMA) transfer (col. 7, lines 8-10).

In regards to claim 11, '239 teaches the system of claim 1 wherein said transport mechanism further comprises: a special core component (Fig. 4—202) configured to receive a YUV decompressed video frame across a VIP bus from said hardware decoder; a PCI core (Fig. 4—401) configured to receive said YUV decompressed video frame from said special core component via a DMA transfer and to send said YUV decompressed video frame to a PCI bus (Fig. 4—402).

3. Claims 14, 16-18, 21-26, 28-32, 34-36, 39-44 and 46-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Gould et al. (US 6,331,852, hereinafter '852).

In regards to claims 14 and 32, '852 teaches a method comprising: decoding live broadcast signals with a decoder (col. 3, lines 57-60; col. 3, line 66-col. 4, line 2); transporting said live broadcast signals to a graphics chip (col. 4, lines 48-52; col. 6, lines 16-20); and rendering a three-dimensional graphics image (col. 4, lines 39-47; col. 5, lines 1-3; col. 5, line 66-col. 6, line 1; col. 6, lines 35-38) on an output device (col. 3, lines 36-40) using said live broadcast signals

In regards to claims 16 and 34, '852 teaches the method of claim 14 wherein said step of transporting comprises, using a PCI bus (col. 3, lines 32-33).

In regards to claims 17 and 35, '852 teaches the method of claim 14 wherein said output device is a television set (col. 3, lines 40-41).

In regards to claim 18 and 36, '852 teaches the method of claim 14 wherein said output device is a monitor (col. 3, lines 40-41).

In regards to claims 21 and 39, '852 teaches the method of claim 15, further comprising: determining if a user interface (UI) event has occurred; and performing a three-dimensional graphics operation, if said UI event has occurred (Fig. 4; col. 6, lines 29-39).

In regards to claims 22 and 40, '852 teaches the method of claim 21 wherein said UI event comprises a changing of a television channel (col. 7, lines 1-8).

In regards to claims 23 and 41, '852 teaches the method of claim 21 wherein said UI event comprises a pausing of a live or a recorded television show (col. 6, lines 33-39).

In regards to claims 24 and 42, '852 teaches the method of claim 21 wherein said UI event comprises initiating a menu or a program guide (col. 6, lines 33-39).

In regards to claims 25 and 43, '852 teaches the method of claim 21 wherein said UI event providing input to a television set or a set-top box (Fig. 1—12 & 16; col. 6, lines 33-34; col. 7, lines 1-4).

In regards to claims 26 and 44, '852 teaches the method of claim 21 wherein said three-dimensional graphics operation comprises a rotation of a three-dimensional graphics frame (col. 8, lines 22-25).

In regards to claims 28 and 46, '852 teaches the method of claim 21 wherein said three-dimensional graphics operation comprises a warping effect (col. 6, lines 55-57).

In regards to claims 29 and 47, '852 teaches the method of claim 21 wherein said three-dimensional graphics operation comprises a surface mapping (col. 7, lines 28-30).

In regards to claims 30 and 48, '852 teaches the method of claim 21 wherein said three-dimensional graphics operation comprises a motion blur (col. 6, lines 53-55).

In regards to claims 31 and 49, '852 teaches the method of claim 21 wherein said three-dimensional graphics operation comprises an operation performed in a three-dimensional graphics environment (Fig. 4; col. 6, lines 61-67).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ezer et al. ('239) in view of Suen et al. (US 6,552,750, hereinafter '750).

'239 teaches the limitations of claim 1 for the reasons above.

In regards to claim 2, '239 teaches a processing unit and/or a video graphics engine that cause a transition between live video and a three-dimensional menu to occur, but fails to teach a synchronization mechanism that synchronizes the output of the video frames and the three-dimensional graphics frames.

In analogous art, '750 teaches a system that receives both video signals and graphics signals at a decoder, decoded and then transferred to a synchronization circuit. The synchronization circuit uses a clock signal in order to synchronize the video and graphics signals to function with the same timing (col. 3, lines 1-2; col. 3, line 65-col. 4, line 10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of '239 to include a synchronization mechanism in order to correctly synchronize the video and graphics signals to the same rate that the television display accepts, thus causing the horizontal and vertical synchronization signals of each of the two streams of data which are used to determine

the beginning of each horizontal and vertical sweep of the display to occur together (col. 4, lines 14-18 & 22-26).

In regards to claim 6, '239 teaches a processing unit and/or a video graphics engine that cause a transition between live video and a three-dimensional menu to occur, but fails to teach a synchronization mechanism that synchronizes the output of the video frames and the three-dimensional graphics frames, and ensures that the output of the video and graphics frames is at a rate of approximately thirty frames per second.

In analogous art, '750 teaches a synchronization circuit that synchronizes video and graphics data to a display rate of 29.97 frames per second, and can be different rates for different formats (col. 4, lines 11-26).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of '239 to include a synchronization mechanism that ensures the video and graphics frames are at a rate of approximately thirty frames per second in order to allow both to be displayed on the display device that requires the specific rate (col. 4, lines 15-18), and to cause the horizontal and vertical synchronization signals of each of the two streams of data which are used to determine the beginning of each horizontal and vertical sweep of the display to occur together (col. 4, lines 14-18 & 22-26).

6. Claims 1 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ezer et al. (US 6,275,239, hereinafter '239) in view of Smith ("VHDL & Verilog Compared & Contrasted").

'239 teaches the limitations of claims 1 and 11 for the reasons above.

In regards to claim 12, '239 teaches a host processor that provides a portable high performance applications platform with a complete high level language development environment ('239—col. 6, lines 52-54), but fails to teach the special core component of the transport mechanism is written in a hardware definition language.

In analogous art, Smith teaches two industry standard hardware description languages, VHDL and Verilog.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of '239 to write the special core component in a hardware definition language since it was known in the art at the time the invention was made that hardware description languages are used to design and simulate hardware behavior and structure, such as processors and chips (Smith—page 771, sections 2 & 3; subsection "Data Types").

In regards to claim 13, '239 teaches a host processor that provides a portable high performance applications platform with a complete high level language development environment ('239—col. 6, lines 52-54), but fails to specifically teach the special core component of the transport mechanism is written in the hardware definition language Verilog.

In analogous art, Smith teaches two industry standard hardware description languages, VHDL and Verilog. According to Smith, Verilog became the IEEE standard 1364 in December 1995 (page 771, sections 1 & 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of '852, in view of '239, to include Verilog as the hardware description language for the processor since it is one of the two industry standard hardware description languages, and the Verilog data types are very simple and are geared towards modeling hardware structure as opposed to abstract hardware modeling (Smith—page 771, sections 2 & 3; subsection "Data Types").

7. Claims 14, 15, 19, 32, 33 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gould et al. ('852) in view of Iacobelli et al. (US 6,919,929, hereinafter '929).

'852 teaches the limitations of claims 14 and 32 for the reasons above.

In regards to claims 15 and 33, '852 teaches a processing unit and/or a video graphics engine that cause a transition between live video and a three-dimensional menu to occur, but fails to teach synchronizing an output of said live broadcast signals from said decoder with an output of a three-dimensional graphics frame from said graphics chip.

In analogous art, '929 teaches a system and method for displaying video and graphics data of different formats onto the same display. A mixer aligns a first media type, video, and incoming data, graphics, to the same format. A signal is then asserted in order to synchronize graphic and video to the same frame or field (Figs. 5A & 5B; col. 5, lines 53-55; col. 11, lines 1-7).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of '852 to include synchronizing the output of

the live broadcast signals from a decoder with the graphics in order to simultaneously display the graphics with the video, since the incoming graphics stream must be synchronized with the video data to have the same output timing rates (col. 1, lines 28-32; col. 2, lines 37-38).

In regards to claims 19 and 37, '852 teaches a processing unit and/or a video graphics engine that cause a transition between live video and a three-dimensional menu to occur, but fails to teach a synchronization mechanism that synchronizes the output of the video frames and the three-dimensional graphics frames, and ensures that the output of the video and graphics frames is at a rate of thirty frames per second.

In analogous art, '929 teaches a system and method for displaying video and graphics data of different formats onto the same display. A mixer aligns a first media type, video, and incoming data, graphics, to the same format. The video interface supports progressive mode, where the frame rate is 30 frames per second. The progressive mode of operation must be programmed into both the graphics and video subsystems. A signal is then asserted in order to synchronize graphics and video subsystems to the same frame or field (Figs. 5A & 5B; col. 5, lines 53-55; col. 11, lines 1-7).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of '852 to include a synchronization mechanism that ensures the video and graphics frames are at a rate of thirty frames per second in order to simultaneously display the graphics with the video, since the

incoming graphics stream must be synchronized with the video data to have the same output timing rates (col. 1, lines 28-32; col. 2, lines 37-38).

8. Claims 14, 20, 32 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gould et al. ('852) in view of Ezer et al. (US 6,275,239, hereinafter '239).

'852 teaches the limitations of claims 14 and 32 for the reasons above.

In regards to claims 20 and 38, '852 teaches a transport mechanism that transports frames from the decoder to the texture memory, but fails to teach using a direct memory address (DMA) transfer.

In analogous art, '239 teaches using a direct memory access (DMA) engine which transfers data between memory buffers and I/O interfaces, such as a digital signal processor and a PCI host bus interface (Fig. 4—403 & 404; col. 3, lines 35-37).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of '852 to use direct memory access to transport the frames from the decoder to the texture memory in order to allow the transfer of data between memory buffers and I/O interfaces, including video and audio input and peripheral interfaces for control and data (col. 3, lines 36-39).

9. Claims 14, 27, 32 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gould et al. ('852).

'852 teaches the limitations of claims 14 and 32 for the reasons above.

In regards to claims 27 and 45, '852 teaches using various visual effects to enhance the video display, therefor it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of '852 to use shatter effect since the examiner takes Official Notice of the fact that it is known to use shatter effect to enhance a video image operation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelton Austin whose telephone number is (571) 272-9385. The examiner can normally be reached on Monday through Thursday from 7:30-5:00. The examiner can also be reached on alternate Fridays from 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Stucker whose telephone number is (571) 272-0911, can be reached on Monday through Thursday from 7:30-5:00. The supervisor can also be reached on alternate Fridays from 7:30-4:00. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEFFREY STUCKER
SUPERVISORY PATENT EXAMINER

Shelton Austin
1/3/2007

SA